CLAIMS

What is claimed is:

1. A sense amplifier, comprising:

a regenerative latch;

an input differential pair of transistors coupled to the regenerative latch; and

a leakage device coupled to each of the transistors comprising the input differential pair of transistors, said leakage device adapted to maintain the input differential pair of transistors in an on state during a pre-charge phase.

2. The sense amplifier of claim 1 wherein the leakage device comprises a field effect transistor.

3. The sense amplifier of claim 1 further comprising a clocked buffer coupled to outputs of the regenerative latch, the clocked buffer providing additional drive current for the sense amplifier.

4. The sense amplifier of claim 1 further comprising a secondary hold latch coupled to outputs of the regenerative latch to maintain an output decision for the sense amplifier while other portions of the sense amplifier pre-charge.

5. The sense amplifier of claim 4 further comprising a pass gate coupling and isolation circuit coupled between the regenerative latch and the secondary hold latch to isolate the regenerative latch from the secondary hold latch.

6. The sense amplifier of claim 1 further comprising a pair of clocking transistors coupled to drain connections of the input differential pair of transistors and the source connections of the input differential pair of transistors is grounded.

7. The sense amplifier of claim 1 further comprising a second pair of input differential transistors, and the sense amplifier further comprises a plurality of clocking transistors, wherein a pair of the clocking transistor couples to drain connections of one pair of input differential transistors and another clocking transistor couples to the source connection of another input differential pair of transistors.

8. The sense amplifier of claim 1 further comprising a second regenerative latch, and the input differential pair of transistors is shared between both regenerative latches.

9. A sense amplifier, comprising:

a regenerative latch having outputs;

an input differential pair of transistors coupled to the regenerative latch; and

a clocked buffer coupled to the outputs of the regenerative latch, the clocked buffer providing additional drive current for the sense amplifier and being clocked by a clock signal that controls the regenerative latch.

10. The sense amplifier of claim 9 further comprising a secondary hold latch coupled to the outputs of the regenerative latch to maintain an output decision for the sense amplifier while other portions of the sense amplifier pre-charge.

11. The sense amplifier of claim 10 further comprising a pass gate coupling and isolation circuit coupled between the regenerative latch and the secondary hold latch to isolate the regenerative latch from the secondary hold latch.

12. The sense amplifier of claim 9 further comprising a pair of clocking transistors coupled to drain connections of the input differential pair of transistors and the source connections of the input differential pair of transistors is grounded.

13. The sense amplifier of claim 9 further comprising a second pair of input differential transistors, and the sense amplifier further comprises a plurality of clocking transistors, wherein a pair of the clocking transistor couples to drain connections of one pair of input differential transistors and another clocking transistor couples to the source connection of another input differential pair of transistors.

14. The sense amplifier of claim 9 further comprising a second regenerative latch, and the input differential pair of transistors is shared between both regenerative latches.

15. A sense amplifier, comprising:

a regenerative latch having outputs;

an input differential pair of transistors coupled to the regenerative latch; and

a secondary hold latch coupled to the outputs of the regenerative latch to maintain an output decision for the sense amplifier while other portions of the sense amplifier pre-charge.

16. The sense amplifier of claim 15 further comprising a pass gate coupling and isolation circuit coupled between the regenerative latch and the secondary hold latch to isolate the regenerative latch from the secondary hold latch.

17. The sense amplifier of claim 15 further comprising a pair of clocking transistors coupled to drain connections of the input differential pair of transistors and the source connections of the input differential pair of transistors is grounded.

18. The sense amplifier of claim 15 further comprising a second pair of input differential transistors, and the sense amplifier further comprises a plurality of clocking transistors, wherein a pair of the clocking transistor couples to drain connections of one pair of input differential transistors and another clocking transistor couples to the source connection of another input differential pair of transistors.

19. The sense amplifier of claim 15 further comprising a second regenerative latch, and the input differential pair of transistors is shared between both regenerative latches.

20. A method of deciding a voltage level of a communication symbol in a sense amplifier, comprising:

performing a pre-charge phase;

performing an evaluate phase in which an input symbol is resolved; and

maintaining an input differential transistor pair in an on state during the pre-charge phase.

21. The method of claim 20 further comprising generating additional drive current for the sense amplifier by operating a clocked buffer coupled to outputs of a regenerative latch in the sense amplifier.

22. The method of claim 20 further comprising maintaining an output decision for the sense amplifier while other portions of the sense amplifier pre-charge.

23. A method of deciding a voltage level of a communication symbol in a sense amplifier, comprising:

performing a pre-charge phase;

performing an evaluate phase in which an input symbol is resolved; and

generating additional drive current for the sense amplifier by operating a clocked buffer coupled to outputs of a regenerative latch in the sense amplifier.

24. The method of claim 23 further comprising maintaining an output decision for the sense amplifier while other portions of the sense amplifier pre-charge.

25. A method of deciding a voltage level of a communication symbol in a sense amplifier, comprising:

performing a pre-charge phase;

performing an evaluate phase in which an input symbol is resolved; and

maintaining an output decision for the sense amplifier while other portions of the sense amplifier pre-charge.